Vladimir Milovanović

PhD, IEEE Senior Member

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PERSONAL INFORMATION

Date of Birth	October 2, 1981
Nationality	Serbian
Marital Status	Married

RESEARCH INTERESTS AND COMPETENCES

Design, modeling and optimization of CMOS and BiCMOS analog, mixed-signal and digital integrated circuits, devices and systems (SoCs), as well as development and implementation of energy-efficient communication, control, machine learning and signal processing algorithms.

EDUCATION AND WORK EXPERIENCE

2021–present *Associate Professor*, Faculty of Engineering, **University of Kragujevac**, Kragujevac, Serbia.

2015–2021 *Assistant Professor*, Faculty of Engineering, **University of Kragujevac**, Kragujevac, Serbia.
Department of Electrical Engineering and Computer Sciences and the Center for Integrated Systems

2015–present *Principal Engineer of Integrated Circuits and Systems on Chip*, **NOVELIC**, Belgrade, Serbia.
Part-Time position — Leading an IC design team on design services and internal development projects

2014–2015 *Postdoctoral Scholar*, **University of California, Berkeley**, United States.
Department of Electrical Engineering and Computer Sciences, Berkeley Wireless Research Center
– Flexible Arrays of Digital and Efficient Radios (FADER/eWallpaper), project funded by DARPA

2011–2014 *Postdoctoral Research Fellow*, **Vienna University of Technology**, Austria.
Faculty of Electrical Engineering, Institute of Electrodynamics, Microwave and Circuit Engineering
– Powerline Communication Systems in Nanometer CMOS Technology, project funded by Lantiq A

2010–2011 *Postdoctoral Researcher*, **Delft University of Technology**, the Netherlands.
Faculty of Electrical Engineering, Department of Microelectronics and Computer Engineering
– Device simulations for LDMOS development, project funded by NXP Semiconductors

2006–2010 *Graduate Researcher / PhD Student*, **Delft University of Technology**, the Netherlands.
Faculty of Electrical Engineering, Department of Microelectronics and Computer Engineering
Delft Institute of Microsystems and Nanoelectronics (DIMES)
- PhD dissertation: *Advanced Breakdown Modeling for Solid-State Circuit Design*
  - research funded by: Texas Instruments Inc. in Dallas, and the Compact Model Council (CMC)

2005–2006 *Design Engineer*, **Radiosoft / Signum Concepts Inc.**, Belgrade, Serbia.
Development of FPGA-based high-speed embedded digital signal processing solutions (SDR modems)

2000–2005 *Dipl.-Ing. Degree*, **University of Belgrade**, Serbia.
Faculty of Electrical Engineering, Department of Electronics
- Diploma thesis: *FPGA Implementation of Bioinformatic Algorithms for Security Purposes*
- Grade Point Average: 9.81 (highest in the generation among more than a thousand students)
  - GPA is on a scale from 6.0 to 10.0 with 6 being the lowest and 10 being the highest mark
- Spring 2005 – The work that lead to the diploma/master's thesis was accomplished at the Department of Electronic Engineering, Faculty of Telecommunication Engineering, Technical University of Madrid (Universidad Politécnica de Madrid, UPM), Spain.
- Summer 2004 – Undergraduate Researcher at the Signal and Image Processing Laboratory, Department of Electrical Engineering, Technion – Israel Institute of Technology, Haifa.

AWARDS

2014 Recipient of the IEEE MIEL's Best Paper Award

2009 Recipient of the IEEE BCTM's Best Student Paper Award

2005 Valedictorian – the best student among his graduating class, University of Belgrade

RELEVANT EXPERTISE

@Uni KG Establishing B.Sc., M.Sc. and Ph.D. curricula in electrical engineering and computer science
Co-Formed the Department of Electrical Engineering and the Center for Integrated Systems
Teaching: Electronics, IC design, Fundamentals of Programming as well as ML/AI courses
Research: Radars-on-Chip, radar signal processing accelerators, mostly shared with NOVELIC

@NOVELIC Formed and acting as team-lead of Digital/Mixed-Signal IC and SoC group of seven engineers
Participated in and lead numerous commercial design services projects for various customers
Internal Radar-on-Chip development for mm-wave integrated radar sensors front- & back-end

@UC Berkeley Mostly worked within the scope of the eWallpaper/FADER research project. The goal was to design a massive MIMO communication platform based on an antenna array with large element count (e.g., hundreds) and utilize beamforming to reduce the interference.

Main Project In charge of synchronization between multiple chips which is accomplished by distributing a common low frequency reference clock to every chip. This clock is then multiplied by means of an Integer-N Bang-Bang Digital PLL. The PLL utilizes a ring-based DCO, and it is completely composed from standard cells thus being fully synthesizable. Its novel architecture utilizes pseudorandom fractional dithering (instead of a $\Delta\Sigma$ modulator dithering) to eliminate any spurious tones in the PSD while preserving superb period-jitter performance. PLL's RTL code as well as the DCO are fully parametric and all PLL constants are soft-programmable. Hence the design can easily be tailored to different needs. The complete PLL was implemented in 28 nm UTBB FDSOI CMOS process technology.

Side Projects Participated on other projects by designing continuous-time and dynamic comparators, sense-amplifiers, operational amplifiers, self-biased amplifiers, LNA/LNTA, chip sign-offs,...

SKILLS

Software/OS UNIX-like Operating Systems: GNU/Linux, BSD-based; Git – distributed revision control

HDLs Verilog(-A/AMS), VHDL(-AMS), SystemVerilog, SystemC, Bluespec, Chisel, MyHDL, HLS

Programming
- Assembly — x86 & x86-64, ARM, PIC, MSP430, TMS320 DSPs (CCStudio)
- Compiled — C/C++/C#, Java, Scala, Pascal
- Markup — TEX, LATEX, (X)HTML (with CSS), XML
- Scripting — bash, ECMAScript, MATLAB/Octave, PHP, Python, Tcl

Paradigms Assembly, Functional, Imperative, Markup, Object-Oriented, Procedural, Scripting, regexp

Design Flows Analog/Digital/Mixed-Signal IC Design Flows based on Cadence and Synopsys CAD tools

Simulators
- Circuit — SPICE-based (HSPICE, SmartSpice, etc.), Spectre, Eldo, ADS, Qucs
- Event-Driven — Cadence Incisive (NCSim), Mentor's Modelsim/Questa, Synopsys VCS
- FEM-based — Technology CAD (TCAD), COMSOL Multiphysics

Technologies A dozen of tape-outs in nanometer CMOS technologies (bulk and SOI) down to 28 nm node

Measurements time and frequency domain, on-wafer probing, substrate calibration, microwave up to 67 GHz

LANGUAGES

Serbian	—	mother tongue / native speaker	
English	—	mastery / proficiency	**C2** level
German	—	vantage / upper intermediate	**B2** level
Dutch	—	threshold / intermediate	**B1** level